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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,389	03/12/2004	Amid Hashim	4799/0112PUS1	6042

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	**PAPER NUMBER**
2841	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/798,389	HASHIM ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The request filed on 2/28/07 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 10/798389 is acceptable and a RCE has been established. An Action on the RCE follows.

2. The amendment filed on 1/31/07 has been entered. Applicants have amended the specification, drawings, and claims 1-16 and 30-33. Claims 16-29 are cancelled.

Drawings

3. The amended drawings, filed on 1/31/07, are approved. The objections to the drawings are withdrawn.

Specification

4. The amended specification, filed on 1/31/07, is approved.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-15 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adriaenssens et al. (US 5997358, hereafter Adriaenssens) in view of McClanahan et al. (US 5396397,hereafter McClanahan).

Regarding claim 1, as shown in figures 6 and 7, Adriaenssens discloses an apparatus comprising a modular connector 60 (electrical connector, see abstract) with a printed circuit board 600 (a multilayer circuit board, see abstract) including:

(a) Circuit elements 1-3 (wiring pairs 1-3 and circuit traces/vias shown in the figure 7B, col.8:19-43);

(b) a plurality of contacts 634/635/62/61 (terminals, col.6:33-67) mounted on the PCB 600 adapted for contacting conductors of a mating connector 20 (modular plug, figure 1), wherein at least some of the contacts are electrically connected to the circuit elements, and wherein original crosstalk occurs between at least some conductors of the mating connector (see compensating signals, col.2:57-col.3:25);

(c) a first section of the PCB 600 (The dielectric layers having circuit layers 603 formed thereon, clearly shown in figures 7A and 7D, col.7:66-col.8:17);

(d) a second section of the PCB 600 (The dielectric layers having circuit layers 601/602/604/605 formed thereon, clearly shown in figures 7A-7C and 7E-7F, col.7:66-col.8:17), and provided above or below the first section; and

(e) at least one crosstalk compensation element 612 (discrete capacitors, col.8:29) utilizing the first section to provide compensating crosstalk to offset the original crosstalk, wherein the circuit elements are provided in the second section (capacitors are shown on layers 603, see figure 7D).

However, Adriaenssens fails to disclose the first section and the second section of the PCB 600 having a first and second dielectric constant respectively.

McClanahan, as shown in figures 1-5, discloses a multilayer printed circuit board comprising:

(a) a first section (shaded layers, high dielectric field layers, col.4: 39-41) having a first dielectric constant (high DK, all shaded layers are high DK, col.3: 20-42);

(b) a second section of the PCB (unshaded layers – basic substrate insulating layers, col.4: 39-41) having a second DK lower than the first DK (col.4: 13-19), and provided above or below the first section (at least figures 3 and 5 show the high dielectric field layers are either sandwiched between the basic substrate insulating layers or in reversed order).

The teachings from McClanahan are about dividing a circuit board into sections having different dielectric constant to achieve field (field control layers) and circuit isolation (isolating structures) in order to minimize EMI and minimum circuit/environmental interactions and parasitics (col.3:37-52).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the high dielectric field control layers from McClanahan on the PCB of Adriaenssens to make the first section to

have a first dielectric constant (high DK) and the second section to have a second dielectric constant (low DK) in order to minimize EMI and minimum circuit/environmental interactions and parasitics.

Examiner remarks:

Applicants should be noted that the limitation that original cross talk occurs between at least some conductors of the mating connector and that the crosstalk compensation element utilizes the first section to provide compensating crosstalk to offset the original crosstalk is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claims 2-3, as shown in figures 7A-7F, Adriaenssens in view of McClanahan (as discussed in claim 1 above) discloses the first section (dielectric layers 603 are all high DK), which comprises a first laminate including a substrate (the 3 dielectric layers of the center section) having the first DK (high DK) and at least a metal sheet (the circuit pattern, figure 7D) attached to at least one surface of the substrate, and a first prepreg above the first laminate and a second prepreg below the first laminate (the center three dielectric layers are sandwiched by two other dielectric layers, figure 7A).

Regarding claim 4, as shown in figures 7D, Adriaenssens at least one crosstalk compensation element 612 (capacitors) is provided at a metal sheet.

Regarding claim 5, as shown in figures 7A, Adriaenssens discloses the second section (top and bottom layers) includes:

(a) A third prepreg (the top layer having circuit layer 601 formed thereon) above the first prepreg;

(b) a first metal layer 601 (see figure 7B) above the third prepreg;

(c) a fourth prepreg (the bottom layer having circuit layer 605 formed thereon) below the second prepreg; and

(d) a second metal layer 605 (figure 7F) below the fourth prepreg.

Regarding claim 6, as shown in figures 7A-7F, Adriaenssens in view of McClanahan (as discussed in claim 1 above) discloses the third and fourth prepregs having the second DK (low DK - the basic substrate insulating layers).

Regarding claim 7, as shown in figures 7A-7F, Adriaenssens discloses the at least one circuit element is provided at the first and/or second metal layer (circuit patterns, figures 7B and 7F), and at least a portion of the at least one crosstalk compensation element is provided at a metal sheet and/or the substrate of the first laminate (figure 7D).

Regarding claim 8, as shown in figures 7A-7F, Adriaenssens in view of McClanahan (as discussed in claim 1 above) discloses a second laminate (the top wiring substrate having circuit layer 601 formed thereon) above the first prepreg; and a third laminate (the bottom wiring substrate having circuit layer 605 formed thereon) below the second prepreg, wherein the second and third laminates have the second DK (the basic substrate insulating layers).

Regarding claim 9, at least as shown in figures 7A, 7B, and 7F, Adriaenssens discloses each of the second and third laminates includes a dielectric material substrate

and at least a metal sheet (the dielectric layer having circuit patterns shown in figures 7B and 7E) on the substrate.

Regarding claim 10, at least as shown in figures 7A, 7B, 7D, and 7F, Adriaenssens discloses the at least one circuit element is provided at the single metal sheet of the second and/or third laminate (figures 7B, 7E), and at least a portion of the at least one crosstalk compensation element (capacitors) is provided at a metal sheet and/or the substrate of the first laminate (figure 7D).

Regarding claims 11-12, as discussed in claims 1 and 2, Adriaenssens in view of McClanahan (discussed in claim 1 above) discloses section 2 as the outer layers sandwiched section 1 in the middle having crosstalk compensation elements formed therein. However, as shown in figure 10, Adriaenssens also discloses an alternate circuit board in which the crosstalk compensation elements are formed on the surface of the circuit board instead. In other words, the structure shown in figure 10 is in reversed order of the structure shown in figure 7A or the structure shown in figure 7A is rearranged to have layers of section 2 being sandwiched by layers of section 1 (high DK layers sandwiched low DK layers in middle of the circuit board). Thus, the final product in such the rearrangement resulting circuit board 1000 (col.9:39-57) includes:

(a) a first laminate (the center layer) including a substrate having the second DK (low DK), and a metal sheet attached to at least one surface of the substrate;

(b) a first prepreg also having the second DK above the first laminate;

(c) a second prepreg also having the second DK below the first laminate.

Examiner remarks: McClanahan also discloses structures (figures 3, 7 and 8) having high DK layers sandwiched low DK layers. And, the arrangement is merely a matter of choice (col.3:53-61).

Regarding claim 13, as shown in figure 10 and 7A, Adriaenssens in view of McClanahan discloses the first section, which includes:

(a) A third prepreg (the top layer shown in figure 10) above the first prepreg;

(b) a first metal layer (the conductive layer) above the third prepreg;

(c) a fourth prepreg (the bottom layer shown in figure 10) below the second prepreg; and

(d) a second metal layer (a conductive layer) below the fourth prepreg.

Regarding claim 14, as shown in figure 10, McClanahan discloses the third and fourth prepregs having the first DK (shaded layers).

Regarding claim 15, at least as shown in figure 3, Adriaenssens inherently discloses the at least one crosstalk compensation element (the capacitors 1012) is provided at the first and/or second metal layer, and the at least one circuit element (any circuit element, circuit traces/vias for example) is provided at a metal sheet of the first laminate.

Regarding claim 30, Adriaenssens in view of McClanahan discloses every limitation as shown in claim 1 above, but fails to disclose the first DK in the range of 4.0-5.0 and the second DK in the range of 2.5-3.5.

However, McClanahan does disclose that the choice of location and material for dielectric field control layers (and also the basic substrate insulating layers, col.7: 34-50)

is highly dependent on the characteristics of the particular application including; for example, circuit geometry, operating frequencies, power level, and so forth (col.3: 53-62; col.7: 33-50). Thus, it is only a matter of choice depending upon particular applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the first DK in the range of 4.0-5.0 and the second DK in the range of 2.5-3.5 in order to provide a predetermined capacitance for a specific application. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claims 31-32, Adriaenssens discloses the at least one crosstalk compensation element, which includes a plurality of capacitors places at different compensation stages of the PCB (sections O, I, II, III, shown in figures 9 and 10). And, the at least one crosstalk compensation element inherently includes a first capacitor for providing a first phase of compensating crosstalk to offset the original crosstalk and a second capacitor for providing a second phase of compensating crosstalk to offset the original crosstalk.

It is noted that the limitation that the at least one crosstalk compensation element includes a first capacitor for providing a first phase of compensating crosstalk to offset the original crosstalk and a second capacitor for providing a second phase of compensating crosstalk to offset the original crosstalk components is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the

claim distinguishes over the prior art. Furthermore, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ 2d 1647 (1987).

Regarding claim 33, Adriaenssens discloses the modular connector is a modular jack (see figure 6).

Response to Arguments

8. Applicant's arguments, filed on 1/31/07, with respect to claims 1-17 and 30-33 have been considered but are moot in view of the new ground(s) of rejection (Adriaenssens in view of McClanahan).

Remarks, page 10: The argument is about that the last Office action was improperly made final.

The Examiner properly made the last Office action Final, because new limitations had been added to the claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen

TUAN T. DINH
PRIMARY EXAMINER